Annals of Telecommunications (2021) 76:537–543
https://doi.org/10.1007/s12243-021-00837-z

Low-power DSSS transmitter and its VLSI implementation

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Received: 9 June 2020 / Accepted: 15 February 2021 / Published online: 25 March 2021

Abstract
An interesting area of application in wireless data communication is direct-sequence spread spectrum (DSSS). Spread spectrum communication techniques make the signals more robust against interference and jamming. These are based on a concept that narrowband signal is scrambled before transmission in such a way that the signals occupy a much larger part of the radio frequency spectrum. As the digital and the analogue system components are required on the same substrate in today's mixed-signal chips, the DSSS transmitter system is proposed to be implemented in field-programmable gate array (FPGA)–based platforms and application-specific integrated circuits (ASICs). With a low-power very large-scale integration (VLSI) architecture, sophisticated processing of wide-bandwidth DSSS systems can be exploited in FPGAs/ASICs. In this article, binary pseudo-noise (PN) sequences are generated using a low-power linear feedback shift register (LFSR) in order to spread transmit signals extensively. The proposed low-power design of LFSR and DSSS transmitter with implementation results is illustrated in this paper. Dynamic power dissipation of the proposed DSSS transmitter is reduced up to 15% and 15.6% when compared to the conventional LFSR and the Gold code–based systems respectively. The proposed hardware is implemented in 180-nm technology and operates at 15.36-MHz frequency.

Keywords Latches · Linear feedback shift register · Low-power DSSS transmitter · Spread spectrum communication · Field-programmable gate array

1 Introduction

1.1 Direct-sequence spread spectrum

Spread spectrum systems were used primarily by the military in the bigger part of half-century. The extensive demand for wireless networks along with progress in very large-scale integration (VLSI) and signal processing practices has enabled spread spectrum to the forefront of commercial improvement. Since May 1995 during which the Federal Communications Commission released the Industrial, Scientific, and Medical (ISM) bands for direct-sequence and frequency-hopped spread spectrum, many commercial products have arrived at the marketplace [1]. It has the capability to withstand interference in high-interference environments. Code division multiple access (CDMA) spread spectrum systems offer abundant flexibility and capacity for multi-user wireless networking applications. The three appreciated commercial applications of spread spectrum technology are global positioning system (GPS), personal communications systems (PCS), and wireless local area networks (WLANs). The direct-sequence spread spectrum (DSSS) of the CDMA systems with high chip rate enables good channel separation, transmission with low average emission level, and high immunity against external interferers [2].

Direct sequence is the most widely known and understood method of spread spectrum modulation [3]. In spread spectrum communication systems, the information to be transmitted is mixed with pseudo-random code sequence to spread the signal over a larger bandwidth. The exact code sequence is used at the receiver to recover the transmitted data. Assigning a code sequence to a user provides an efficient means of identifying spread spectrum signal related to each user and thus allowing the recognition of various users' signals. Figure 1 presents a block diagram of a DSSS system. Spreading and de-spreading are performed in the baseband region, whereas the band-pass region is used to modulate the coded signal.

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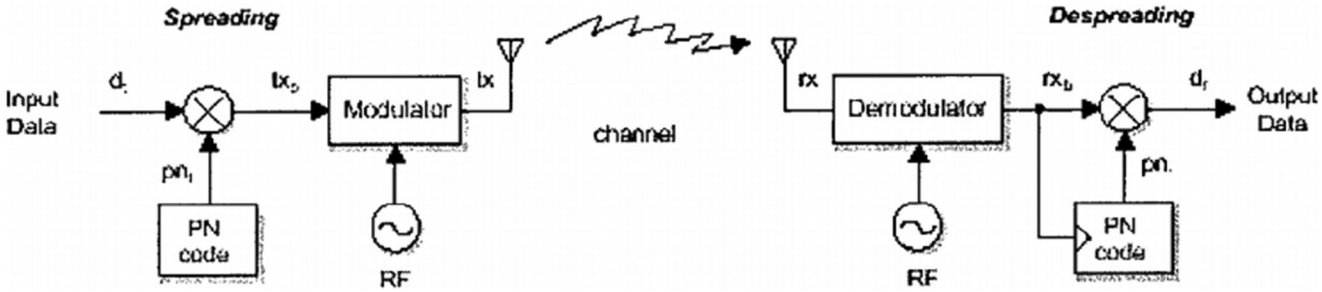


Fig. 1 DSSS system

In this DSSS digital system, input data are digitized before it is combined with code sequence. The pseudo-noise code is generated at the PN sequence generator and it is multiplied with the digitized input signal to achieve spreading. After spreading, the signal is ready to be modulated onto radio frequency (RF) carrier. Then, the transmission is done over the channel. The recovery of the original information is performed at the demodulator and de-spreader modules of the receiving part. One of the characteristics of spread spectrum signals is that the signal cannot be detected by means of a conventional narrowband receiver. Signal recovery can be done in those receivers, which know the proper pseudo-sequence and are able to synchronize their local sequence generators with that being received. The process of de-spreading once again involves multiplication of the spread signal with the PN sequence.

1.2 PN sequence

One of the most commonly used PN sequences in DSSS is maximal length sequences [4]. They are the most widely known binary PN sequences and have excellent autocorrelation properties that make them very useful for general spread spectrum communication systems. By definition, maximal sequences are those sequences that possess the longest codes possible for a given shift register or delay element of given length. PN sequence is balanced wherein in each period, the number of "ones" and the number of "minus ones" differ by exactly one. It is important to note that maximal sequences are linear codes; they are easily decoded and as such should not be used for secure communications. The length of a maximal sequence is governed by the number of shift register stages used in the construction of the generator. If the sequence generator somehow enters the all-zero state, it will remain in that state indefinitely. Linear feedback shift registers make extremely good pseudo-random pattern generators. In Fig. 2, a block diagram of a simple linear feedback shift register is presented. Such generators are composed of a series of shift registers with feedback from even number of taps.

The inputs of linear feedback shift register (LFSR) are linear functions of its previous states. It is a shift register whose input bit is driven by the exclusive OR (XOR) of some bits of the overall shift register value. The initial value of the LFSR is called "seed" which is a non-zero value. The operation of theregister is deterministic since the sequence of values produced by the register is completely determined by its current state. Likewise, the register has a finite number of possible states, and it will eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random when it has a very long cycle. In LFSR, some outputs are combined with exclusive OR configuration to form a feedback mechanism depending on the number of bits it specifies and those outputs are fed back as the inputs to one of the flip-flops, probably the first flip-flop as shown in Fig. 2.

It can be noted that the only signal necessary to generate the test patterns is the clock. When the flip-flops are loaded with the non-zero seed value (zero would cause the LFSR to produce all 0 patterns) and LFSR is clocked, it will generate a pseudo-random pattern of 1s and 0s. It sequences through $2n$-1 states, where n is the number of registers in the LFSR. At each clock edge, the contents of the registers are shifted right by one position. There is a feedback from predefined registers or taps to the leftmost register through an exclusive OR (XOR) gate. For 8-bit LFSR, when taps are $(3, 4, 5, 7)^{th}$ bits, the feedback polynomial is 1+X^3+X^4+X^5+X^7 and its architecture is shown in Fig. 3.

2 Literature review

Due to the inherent property of better noise immunity and other advantages, signal processing for communication systems is performed in modern times almost entirely in the digital domain with high throughput. This requires an efficient modelling and testing of its sub blocks like PN sequence generator, spectrum spreading and de-spreading digital circuits, digital modulators, and demodulator modules that give high throughput. Keeping the high processing speed is another big challenge for developing a DSSS system. Such a design of multistage and low complexity detectors is particularly useful in area constrained applications [5]. Simpler and dedicated hardware circuits can only provide the high-speed processing capability to meet these contrasting requirements [6]. The parallel processing capability of field-programmable gate array (FPGA) makes them ideally

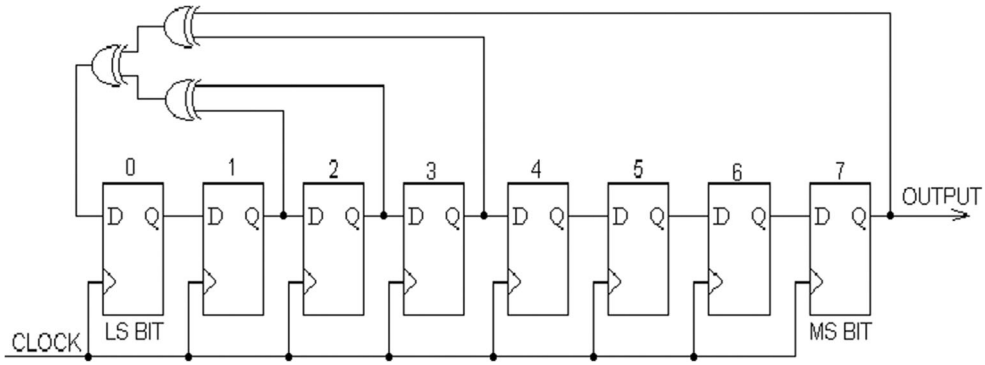


Fig. 2 Linear feedback shift registers

suitable for baseband/radio frequency (RF) digital signal processing in DSSS applications [7]. The hardware which works on the principles of direct-sequence spread spectrum technology must be easy to use, provide better performance, and be highly efficient. High-speed and smaller circuits are always desirable in digital systems that make them suitable for low-power applications with its smaller size [8]. The design solution should also provide high-throughput and high-speed data transfer which can be directly used for providing quality of service to cellular mobile communication [9]. Designs modelled using hardware description language (HDL) often have both speed and area advantages over functionally equivalent software-based designs [10]. The same designs may be implemented for low-power applications with the different approaches through scalable and reconfigurable technology.

LFSR is the key component to provide different sequences needed for spreading the input code. Space-time block codes (ST-BC) have also been used in DSSS systems for producing the hybrid sequences [11]. LFSR architectures are implemented with NAND gates, pass transistors, and transmission gates and the design with pass transistors provides lesser area requirement compared to other two methods [12]. The clock gating technique is used to reduce the power consumption of the linear feedback shift register [13]. Lots of techniques were proposed for area optimization of LFSRs. Among those techniques, the one which reduces the area is multimode architecture for error correcting codes. This technique reduces the hardware complexity up to 49.1%.

The parallel architecture, mainly leads to higher throughput for the designs. There are various techniques in which the design is employed in parallel architecture to increase the device speed. One such architecture is employed in the LFSR design where the area-time product reduces up to 59% compared with other architectures.

The design of high-speed parallel LFSR architecture based on parallel infinite impulse response filter design is also introduced [14] [15] [16]. Its contribution is twofold. The first one is the transformation of serial LFSR architecture into a parallel LFSR architecture. Then, a new formulation is proposed to modify the parallel LFSR to the form of pipelining and retiming algorithm. The parallel transformation achieves a full speed-up compared to serial architecture at the cost of an increase in hardware overhead. The pipelining and retiming algorithms are used to reduce the critical path in the parallel architecture, and it reduces the hardware cost.

All these optimizations are performed at the area or power level separately. The pulsed latch technique used in LFSR optimizes the design in both area and power. This design is applicable to any LFSR architecture and it exhibits the same correlation properties as that of conventional LFSR.

3 Proposed system

The proposed system that implements the transmitting section of DSSS contains a multiplier, low-power LFSR, BPSK modulator, and RF carrier generator.

In the proposed system shown in Fig. 4, the traditional PN sequence generator present in the DSSS transmitter is replaced

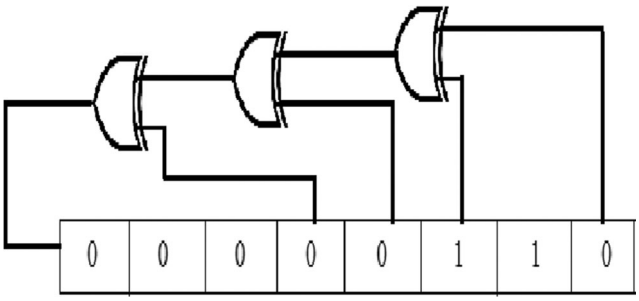


Fig. 3 LFSR for feedback polynomial 1+X^3+X^4+X^5+X^7

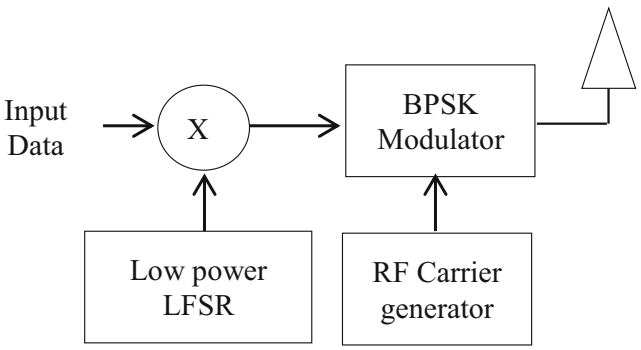


Fig. 4 Proposed low-power LFSR transmitter

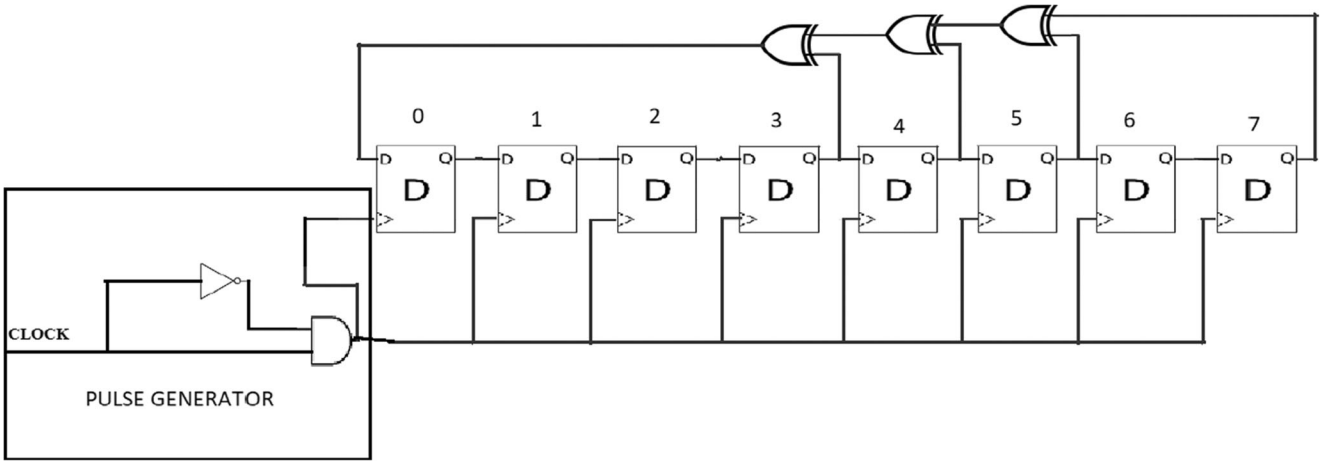


Fig. 5 Proposed low-power LFSR

by a low-power PN sequence generator which is a latch-based LFSR. PN sequence is generated not in response to clock signal but in response to the pulse.

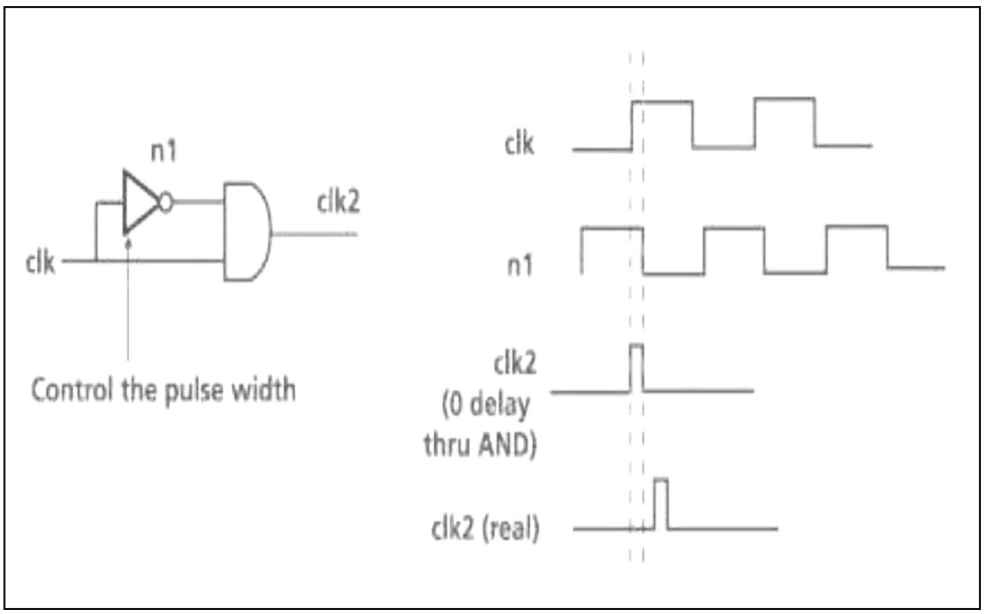
3.1 Low-power LFSR

Commonly, LFSR is formed using a chain of register feedback from two or more taps. LFSR is most often a shift register whose input bit is driven by performing the XOR operation on the outputs of some shift registers. The pulsed LFSR used in the proposed DSSS transmitter is shown in Fig. 5, which contains a pulse generator, D latches, and XOR gates. Individual pulses are generated using the pulse generator and are given to each D latch. When the D latch is triggered using the pulses, the data will start shifting. The values of the tap positions 3, 4, 5, and 7 are taken and given as input to the XOR gates. The values of the 7th and 5th tap position are taken and given as input to the first XOR gate. The output of the first XOR gate and the 4th tap position are given as input to the second XOR gate. And then the output of the second XOR gate and the value of the 3rd tap position are given as the input to the third XOR gate. The output of the third XOR gate is given as the input to the 0th tap position. These connections with non-zero seed value enable all $2n$-1 patterns to be generated successfully. Thus, this system implements 8-bit PN sequence of polynomial 1+x^3+x^5+x^7. This architecture can also be applied during testing methodologies of VLSI circuits [17–20] and for different algorithms used in creating LFSR-based architecture for the random pattern generation [21].

3.2 Pulse generator

Reduction in power dissipation is achieved in LFSR by the use of pulses generated by the pulse generator instead of a

Fig. 6 Pulse generator



a

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
lfsr_pulse	27	1636.523	5059.639	6696.163
u0	3	177.362	540.782	718.144
u1	3	177.362	508.359	685.721
u2	3	177.362	650.750	828.112
u3	3	177.362	419.739	597.101
u4	3	177.362	749.025	926.387
u5	3	177.362	547.713	725.074
u6	3	177.362	500.795	678.157
u7	3	177.362	500.805	678.167
u10	1	72.543	60.328	132.871
u8	1	72.543	75.938	148.480
u9	1	72.543	53.156	125.699
xx0	0	0.000	0.000	0.000

b

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
lfsr	27	1636.523	9908.543	11545.066
u0	3	177.362	1017.938	1195.300
u1	3	177.362	1097.543	1274.905
u2	3	177.362	1015.499	1192.861
u3	3	177.362	982.854	1160.216
u4	3	177.362	1148.122	1325.484
u5	3	177.362	1122.262	1299.624
u6	3	177.362	1081.092	1258.454
u7	3	177.362	1161.749	1339.111
u10	1	72.543	286.360	358.903
u8	1	72.543	154.150	226.693
u9	1	72.543	280.722	353.265

c

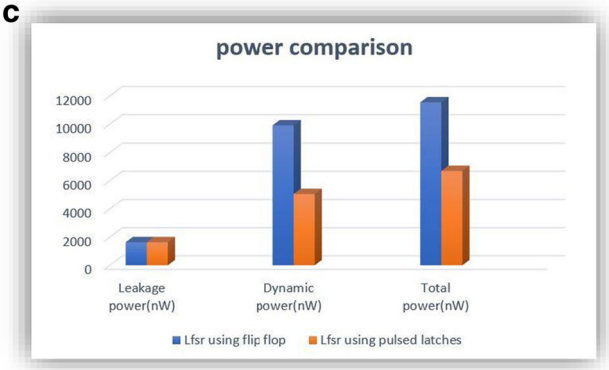


Fig. 7 **a** Power report of LFSR obtained using Cadence. **b** Power report of pulsed latch–based LFSR. **c** Comparison

clock signal. The pulse generation circuit is shown in Fig. 6 which consists of the clock, an inverter, and an AND gate.

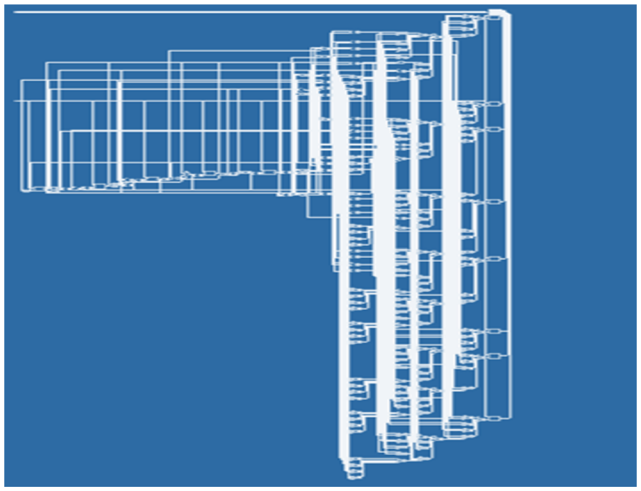


Fig. 8 Schematic of the proposed LFSR

The clock, which is a never-ending pulse train with known frequency, amplitude, and edge rate, is applied at the input of the pulse generator. The generated pulse is used to initiate the propagation of a data signal. The inverter $n1$ used in the pulse generator delays the clock pulse and hence controls the width of the pulse.

4 Experimental results

In this project, the proposed DSSS transmitter with pulsed latch–based LFSR is modelled using very high-speed integrated circuit hardware description language (VHDL) and implemented using industry standard electronic design automation (EDA) tools from Cadence. The implementation is also done on the Xilinx FPGA device xc7z020clg484-1 available in Zedboard.

4.1 PN sequence generators

Design models for conventional LFSR, gold code, and pulsed latch–based LFSR are developed first using VHDL. The simulation of these sequence generators is done using the tool NCsim from Cadence.

After performing the simulation, synthesis of the design is performed to analyze the design parameters of the design. The power result is shown in Fig. 7a, b. The power comparison chart of conventional and proposed LFSR is shown in Fig. 7c. The conventional LFSR consumes a power of 6696 nW and the proposed LFSR consumes a power of 11,545 nW.

From these figures, it is apparent that the proposed LFSR has lesser power consumption compared to conventional LFSR. The reduction in power dissipation is achieved by using the pulsed latches instead of flip-flops. Instead of applying the clock signal for its entire period, a pulse (clk2) which is generated from the clock signal with a very short duration, as

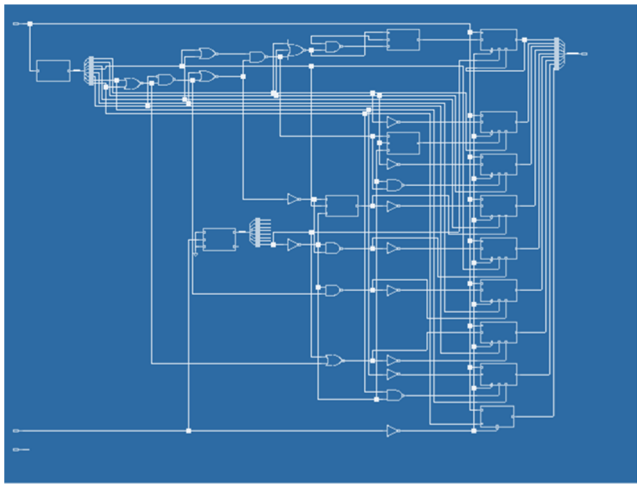


Fig. 9 Schematic of the proposed DSSS transmitter

shown in Fig. 6, is applied to trigger the latches. This limits the duration of clock signal applied to the latches and helps in diminished power dissipation.

4.2 Proposed DSSS transmitter

In this section, the experimental results of the proposed DSSS transmitter are shown and explained. In this work of achieving the spreading, 8-bit PN sequence of polynomial 1+x^3+x^5+x^7 is generated using the pulsed latch LFSR and the data symbol is chopped into several parts following the pseudo-random code. Then, the signal is modulated by a BPSK modulator which makes the signal ready for transmission. This modulation scrambles and spreads the portions of data, and thus the bandwidth of modulated signal size is nearly identical to that of the PN sequence. The chip rate taken in this particular case is 80 Mbits/s, the symbol rate is 500 Kbits/s, and the processing gain is 160. The processing gain can be still made larger by employing a longer PN sequence and more chips per bit, but devices used to generate the PN sequence impose practical limits on the achievable processing gain.

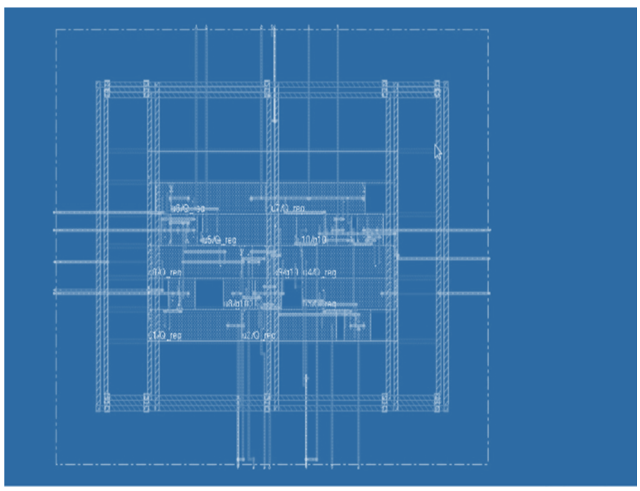


Fig. 10 Layout of DSSS Transmitter

Table 1 Implementation details of the DSSS transmitter

Proposed DSSS implementation parameters	Details
Device	xc7z020clg484-1
Number of LUTs	34 out of 53,200
Number of slice flip-flops	29 out of 106,400
Number of bonded IOs	10 out of 200
Minimum period	65.16ns
Maximum frequency	15.36 MHz

4.3 VLSI implementation

Front-end design entry is done with VHDL. Experimental results are analyzed and evaluated, and results are taken using Cadence tools (NCsim, RTL Compiler and Encounter). GDSII (Graphical Data Stream Information Interchange) file is created in 180-nm technology during VLSI implementation. Figures 8 and 9 show the schematic of the proposed LFSR and DSSS transmitter respectively obtained using the tool RTL compiler from Cadence Systems. These schematics illustrate the multiplexers, gates, and buffers/inverters used in the hardware design and the connections among them.

Placement, Routing, and Timing analysis are performed using Encounter tool and then finally GDSII file is created. Figure 10 shows the layout of the proposed system created from the netlist file and the Standard Design Constraints (SDC) files after synthesis and physical design process. This system can be implemented to fabricate Application-specific integrated circuits for Jammer suppression systems proposed in [22].

4.4 FPGA implementation results

The results obtained after implementing the proposed systems on Xilinx Zynq 7000 FPGA, are shown in the Table 1.

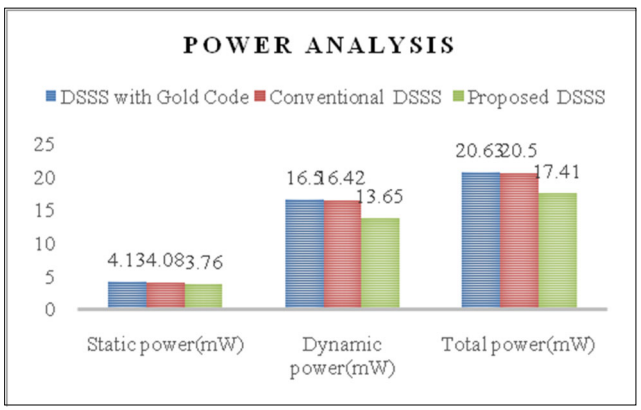


Fig. 11 Power analysis

The authors in [23] used Xilinx Spartan 3 FPGA for developing, testing, and implementing the DSSS transmitter and receiver system. The number of look up tables (LUTs) and flip-flops used in that design are 2541 and 821 respectively.

4.5 Power analysis

From the experimental analysis depicted in Fig. 11, it is observed that the proposed latch-based DSSS transmitter provides a better solution compared to the conventional DSSS transmitter in terms of area and power. This is achieved by replacing the PN sequence generator by means of the pulsed latch–based sequence generator.

5 Conclusion

Since nowadays the systems are becoming more complex that may consume more power, low-power design techniques need to be incorporated in integrated circuits. One such technique proposed for DSSS systems is the pulsed latch–based PN sequence generator. Instead of using flip-flops which are level sensitive, latches are used which are sensitive to edges of the clock signal. An improvement of power dissipation of 15.07% is achieved while using the proposed technique. The implementation of the DSSS transmitter technique in HDL has the advantages that the design is fully reconfigurable. The number of bits and PN sequences can be changed very easily and it is useful for both FPGA and ASIC implementations. The proposed method can be further enhanced by diverse modulation techniques. Different methods for PN sequence generation can also be used for generating the spreading codes. Also, the frequency hopping spread spectrum technique can be used instead of DSSS. It is demonstrated in the article that proposed DSSS systems have lesser power consumption than conventional architectures due to the pulsed latch technique. This low-power version of DSSS will surely help in power reduction when implemented in any communication system that uses the DSSS method of communication.

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